Computational Paradigms for Nanoelectronics
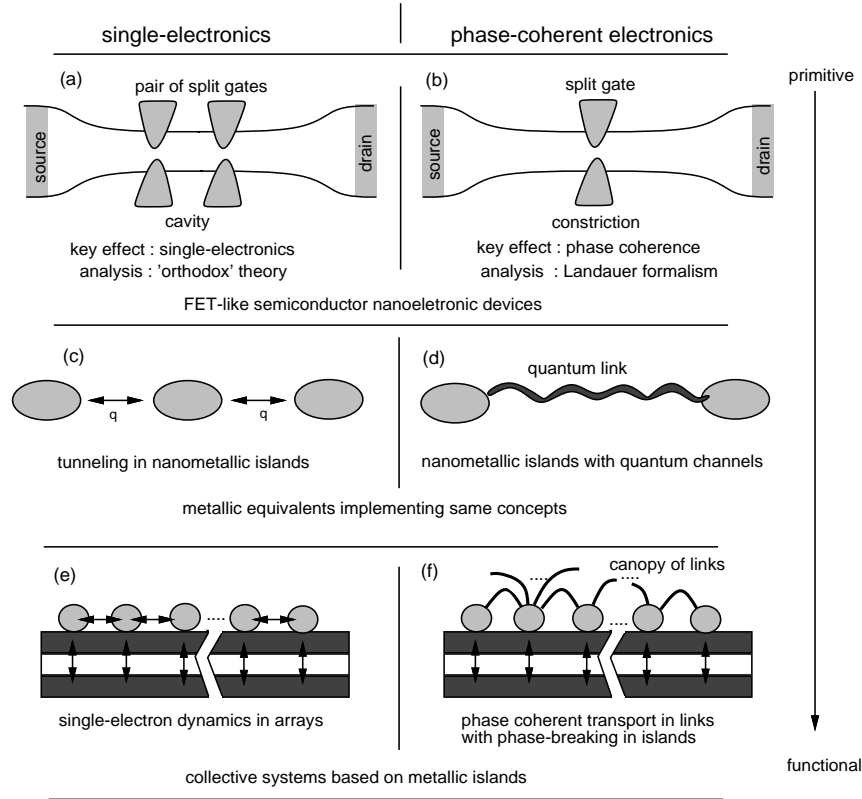
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General Outline

- We provide examples of *collective computation* in networks of nanostructured devices. The special purpose functional device concept adopted here can be contrasted with other approaches which envision the design of general purpose computers on the basis of quantum mechanical logic gates.

- Instead of using *globally coherent quantum systems* to generate computational abilities, we use *semiclassical* global models, as the basis from which to conceive nanoelectronic functional devices. The latter models hold the promise of room temperature operation.

- We make well-defined assumptions concerning the properties of *interconnection networks*. While the functional devices studied here are promising, their practical realizations are crucially dependent on the technological feasibility of these assumptions.
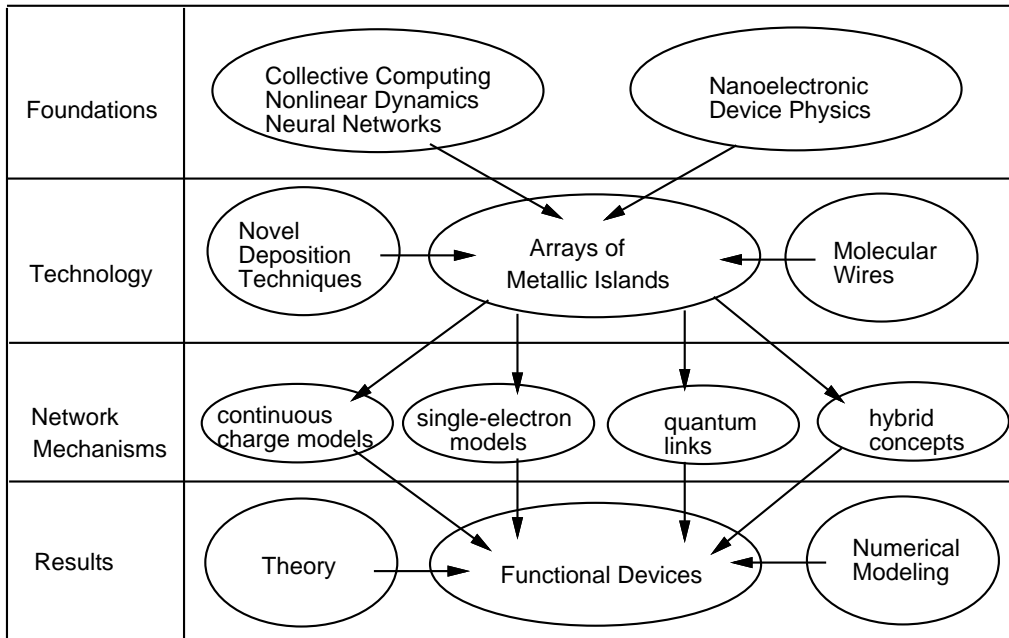
Nanoelectronics:
Primitive To Functional Devices

single-electronics | phase-coherent electronics

(a) pair of split gates
source / drain
cavity
key effect : single-electronics
analysis : 'orthodox' theory

(b) split gate
source / drain
constriction
key effect : phase coherence
analysis : Landauer formalism

primitive

FET-like semiconductor nanoeletronic devices

(c)
q   q
tunneling in nanometallic islands

(d) quantum link
nanometallic islands with quantum channels

metallic equivalents implementing same concepts

(e)
....
single-electron dynamics in arrays

(f) canopy of links
....
phase coherent transport in links
with phase-breaking in islands

functional

collective systems based on metallic islands

A schematic reduction of typical semiconductor realizations of nanoelectronic concepts to collective functional devices based on arrays of metallic islands. Arrays of very small metallic islands can be created by techniques which are not limited by lithography. (a)&(b) MODFET-type semiconductor devices which exhibit single- and phase-coherent electronics at $T \sim 1K$. (c)&(d) Much smaller but similar metallic devices, which have higher operating temperatures either due to low capacitance, or due to the need for phase-coherence only over short distances. (e)&(f) Collective semiclassical systems which can be analyzed, by including quantum effects locally over the tunnel barriers, or on the quantum links.
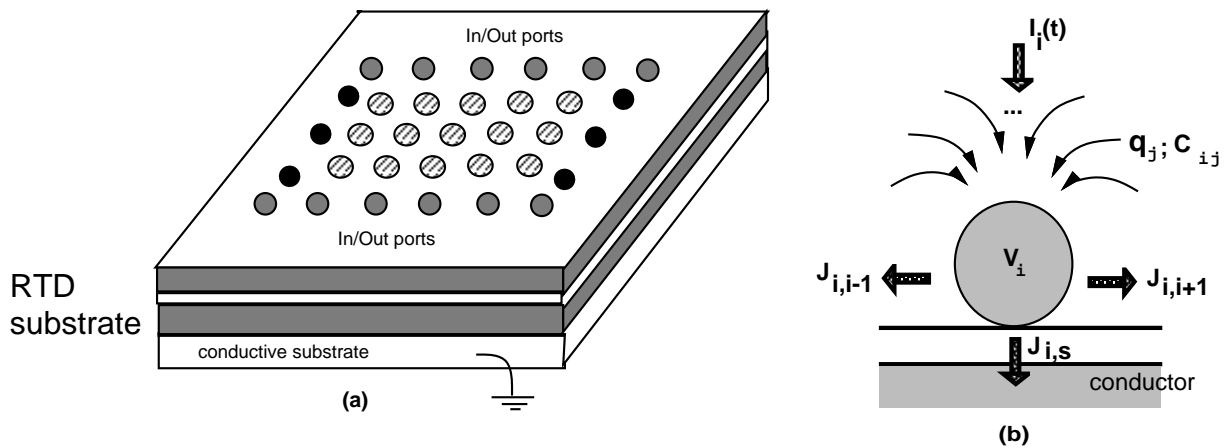
Our Approach to Functional Devices

Foundations	Collective Computing / Nonlinear Dynamics / Neural Networks — Nanoelectronic Device Physics
Technology	Novel Deposition Techniques — Arrays of Metallic Islands — Molecular Wires
Network Mechanisms	continuous charge models — single-electron models — quantum links — hybrid concepts
Results	Theory — Functional Devices — Numerical Modeling

Prototype Networks
of Nanoscale Metallic Islands

An array of metallic clusters on an active semiconductor substrate. Resistive conductive links exist between neighboring clusters, and each cluster is driven by a current source. Non-linear conductive links to the substrate provide the necessary complexity required for cooperative computation.

Summary of Collective Computation
# For Different Transport Mechanisms

| *Network or Transport type*	*Technological Assumptions*	*Theoretical Techniques*	*Example Collective Activity*
continuous charge with resistive (nonlinear) coupling	spatially variable resistances, access to interior nodes	Liapunov stability theory	image processing, associative memory, LOGIC Gates
resonant single-electron tunneling	same as above, and small capacitance C	Liapunov theory and monte carlo simulations	Logic gates, associative memory (breaks down for very small C)
single-electron tunneling	access to interior nodes, and arbitrary choice of capacitances C_{ij}	linear programming	associative memory
single-electron tunneling	same as above	matrix theory and discrete math	combinatorial optimization
phase-coherent	molecular wires	nonlinear dynamics	effort in progress

Summary of key results for systems of large arrays of nanometallic islands with different types of interconnection mechanisms (i.e., different types of transport mechanisms in the arrays).

Example 1: A Two-Node Associative Memory
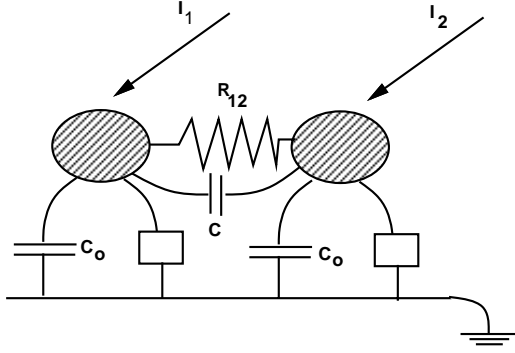
(a) Two node example
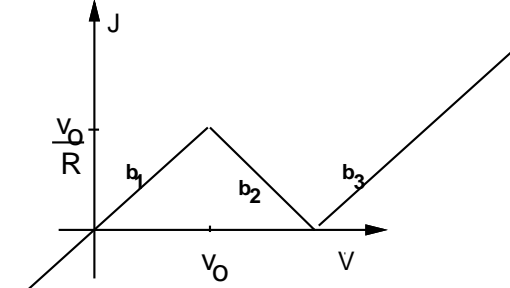
(b) substrate transport function

$$J_s(v) = \begin{cases} v/R & v < v_0 \\ (2v_0 - v)/R & v_0 \leq v \leq 2v_0 \\ (v - 2v_0)/R & v > 2v_0 \end{cases} \tag{1}$$
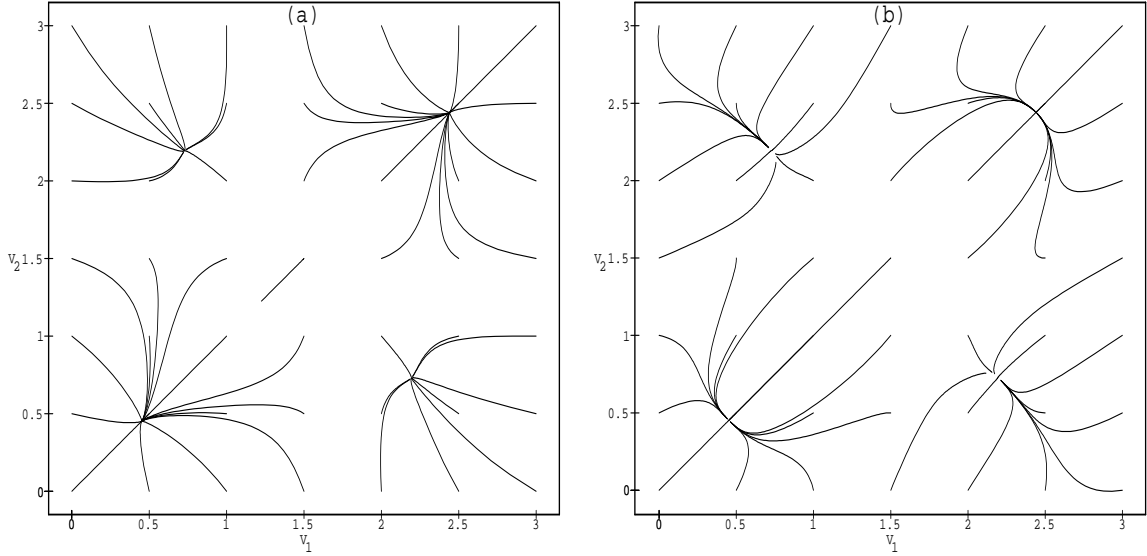
Kirchoff equations describing the dynamics of the two node network can be written as,

$$\begin{bmatrix} C_0 + C & -C \\ -C & C_0 + C \end{bmatrix} \begin{pmatrix} \dot{v}_1 \\ \dot{v}_2 \end{pmatrix} = \frac{1}{R_{12}} \begin{bmatrix} -1 & 1 \\ 1 & -1 \end{bmatrix} \begin{pmatrix} v_1 \\ v_2 \end{pmatrix} - \begin{bmatrix} J_s(v_1) - I_0 \\ J_s(v_2) - I_0 \end{bmatrix}, \tag{2}$$

where, for the sake of analysis, $I_1 = I_2 = I_0$.

Example 1: Phase Portrait : Continuous Model

Phase portrait for two-island system in the continuous-charge model, in which the voltage axes have been scaled with respect to v_0. The parameters are $R_{12} = 5R$, and $I_0 = v_0/2R$. (a) with only substrate capacitance $C_0 = 1$, and (b) with identical mutual and substrate capacitances : $C = C_0$.

- *Equilibrium Points:* Four equilibrium points, or memory points. The actual number of equilibrium points is determined (programmed) by the resistive links.

- *Associative Memory Operation:* If the system is initialized in the state (v_1, v_2), then it evolves to the equilibrium point 'closest' to it.

General Nanometallic Arrays

(a) current-driven network   (b) substrate transport function
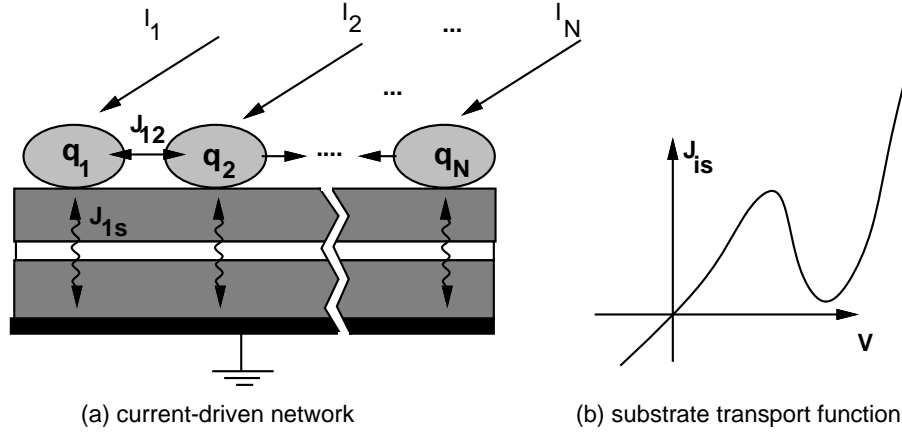
The dynamics of the above one-dimensional array is given by

$$\frac{d}{dt}q_i = C_i\frac{d}{dt}v_i = -\left[J_{is}(v_i) + \sum_{j\neq i} J_{ij}(v_i - v_j)\right] + I_i(t) \qquad (3)$$

where $I_i(t)$ is the driving current, q_i is the charge, v_i is the poten-
tial, and C_i is the capacitance, with the subscript i indicating the
relevant island.

- A non-monotone substrate nonlinearity of the kind shown
  here, is the minimal condition for the realization of collective
  effects.

- The dynamics is similar to the additive short term memory
  (STM) models of neural networks. However, the circuit real-
  izations of the additive STM model involve amplifiers as well
  as a massively interconnected network of resistors.

- We show that, even without amplifiers, and massive connec-
  tivity it is possible to generate nontrivial computational abil-
  ities using equations 3, if certain reasonable nonlinearities are
  permitted to enter the network equations.

Limits to Continuous Models:
Single-Electron Effects

Issues:

- Single electron effects will become pertinent in the nanometallic networks either due to the lowering of temperature, or due to the physical scaling of the metallic islands down to $d \sim 10nm$ (small capacitance). Devices demonstrating single electron charging at room temperature have been fabricated.

- Single electron effects in the networks can be studied using Monte Carlo techniques.

Conclusions:

Monte Carlo Simulations Show the following:

- For a range of capacitance parameters, the discrete stochastic dynamics (due to single-electron effects) follow the continuous charge models fairly closely. Hence, the collective behavior of the arrays under single-electron effects can be adequately studied using the continuous models.

- If the capacitance parameters become very small, then the discrete dynamics may lead to novel circuit behavior (such as limit cycles).
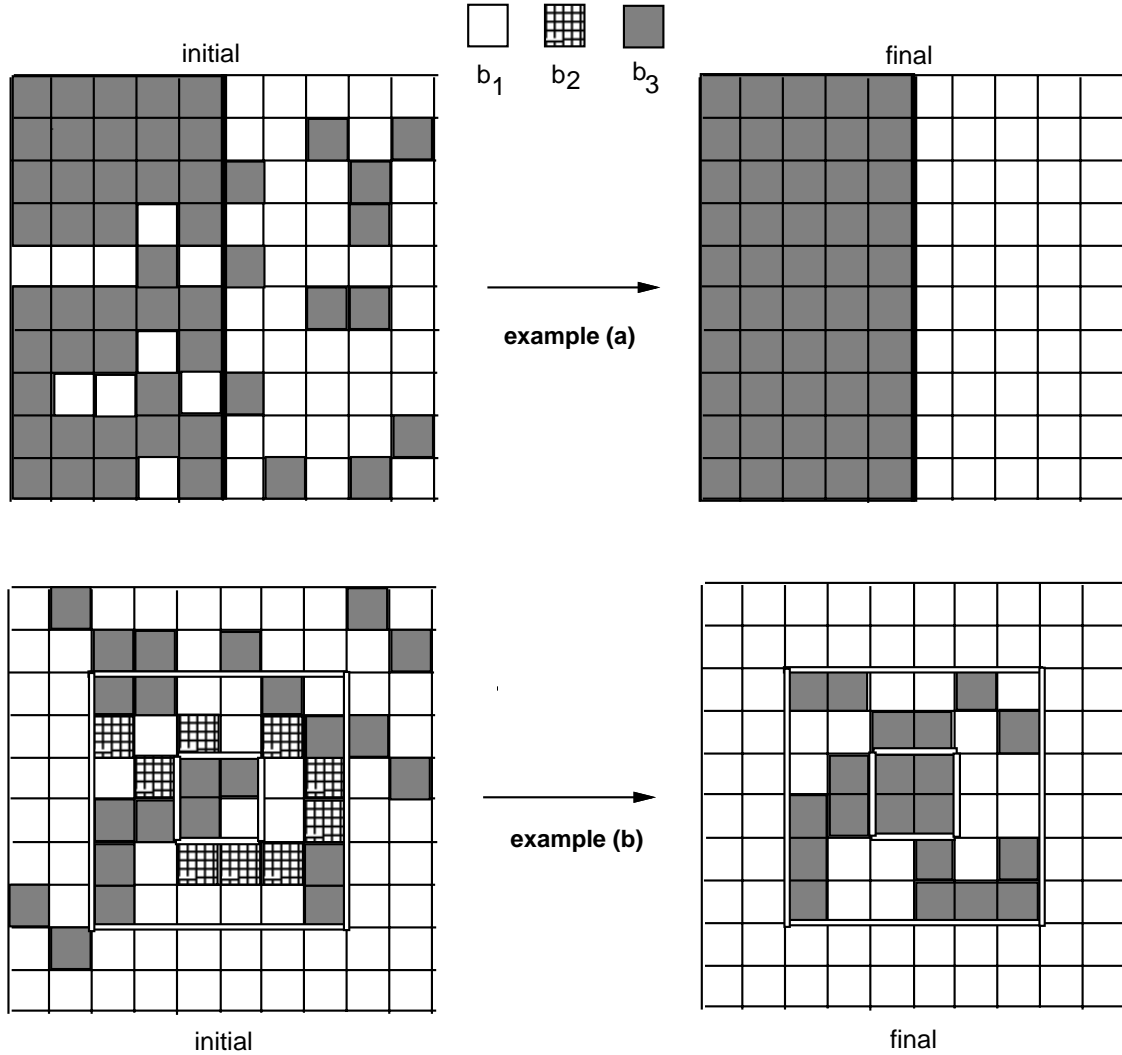
Example 1: Phase Portrait : Single-Electronics
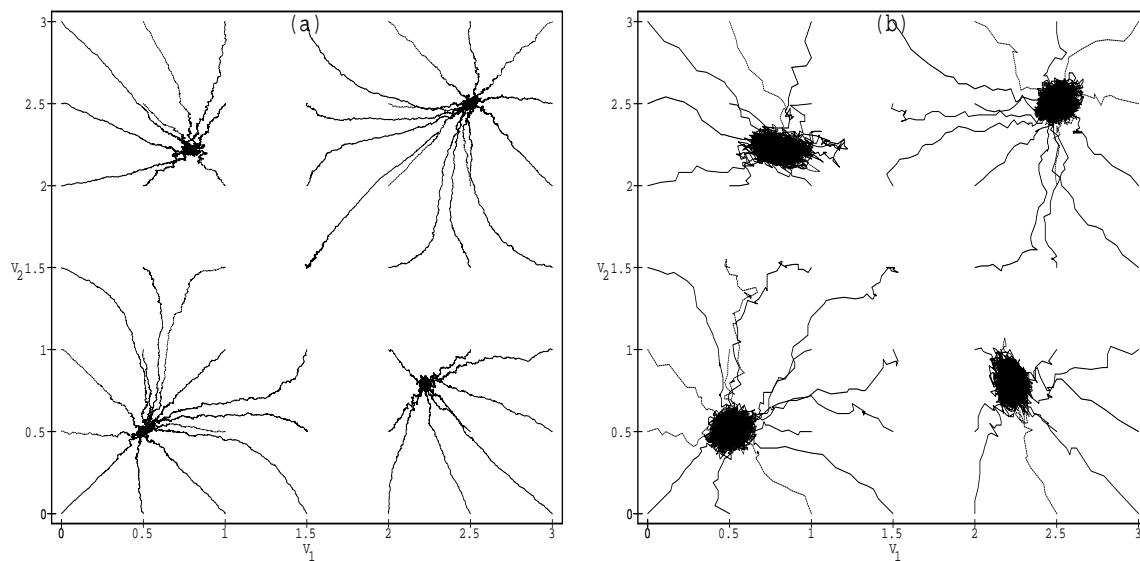
Phase portrait for single-electron stochastic dynamics, with $R_{12} = 5R$, and $I_0 = v_0/2R$. (a) with $\eta = q/C_0 v_0 = 10^{-3}$, $kT = 0$, (b) with $\eta = 10^{-2}$ and $kT = 0$, and

Example 2: Rudimentary Image Processing For both Continuous Charge and Single-Electronics

Rudimentary image processing capability in a *near-neighbor* connected network of 10×10 islands, which are all pumped by the same current $I_0 = v_0/2R$. Each island is colored in accordance with the particular branch - b_1, b_2, or b_3 (as described in the figure for the two-node example) of the substrate nonlinearity, the island potential lies on.

(a) The resistive network is uniform $R_{i\pm1,j\pm1} = 6R$. The input contains domains which are either predominantly black, or white,

and the resulting output recovers domains which are either all black, or all white.

(b) The network is partitioned into three concentric regions. The islands in the outermost and innermost regions are coupled with low resistances $R_{i\pm1,j\pm1} = 3R$, and the islands in the intermediate region are coupled with high resistances $R_{i\pm1,j\pm1} = 13R$. Parts of the network with low resistance produce regions which are either all white, or all black depending on which was predominant in the initial state.

Ising-Type Single-Electron Networks
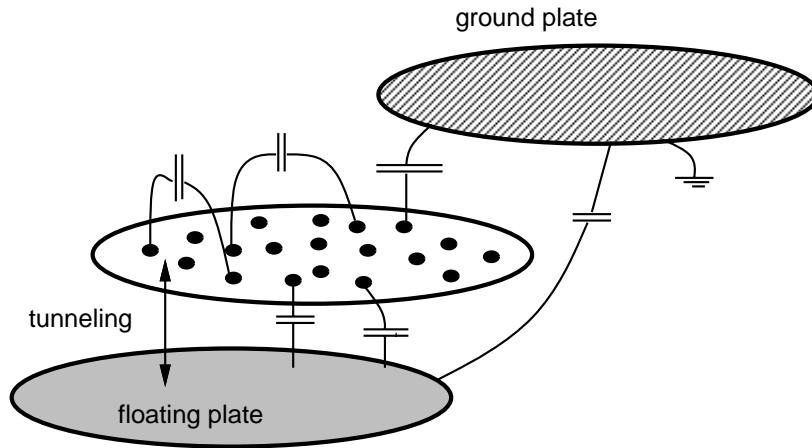
- **Dynamics minimizes a discrete quadratic function.**

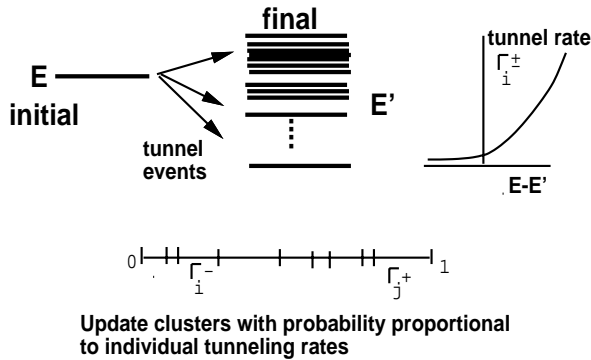$$E(Q) = \frac{1}{2}Q^T \mathcal{C}^{-1} Q \qquad (4)$$

- **Initialize system with charges.**

- **Find minimum energy charge configuration.**

- **Is it a neural network ?**

Single-Electron Networks
Vs. Hopfield Networks

Array of Clusters

●   ...   ●

t :   {n$_1$ ...   n$_N$}

at time t, there are n$_i$ electrons on each of the N clusters

■ random time steps, chosen by consideration of all tunneling rates.

■ pick next cluster to be updated at random but with probability proportional to individual tunneling rate

tunneling rates :

● ●   .....   ●

■ compute initial energy E for the configuration {n$_i$} at time t

■ for N clusters, 2N different tunneling events are possible

■ compute new energy E' for each of the tunneling events

final

E initial —

E'

tunnel events

tunnel rate Γ$_i^\pm$

E-E'

0 |— Γ$_i^-$ —————— Γ$_j^+$ —| 1

Update clusters with probability proportional to individual tunneling rates

Hopfield Model

●   ...   ●

t :   {S$_1$ ...   S$_N$}

at time t spins S$_i$ = ±1 are present at the n nodes

■ update spins at uniform time intervals

■ select particular nodes at random and flip its spin with probability determined by the Fermi-Dirac distribution

flipping probability

determine energy H of the initial spin configuration {S$_i$} at time t

determine energy H' after spin k is reversed

proceed with the reversal of spin k, with probability given by the Fermi-Dirac function :

F-D

H-H'
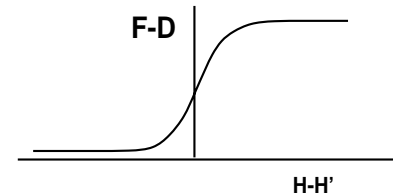
The integer number n_i of electrons present on an island, and the spin variable $S_i = \pm 1$ are corresponding variables. The energy E of the cluster network is a quadratic function of the n_i's, with coefficients C_{ij}. Certain configurations of the n_i will minimize this energy. Likewise the energy H of the Hopfield network is minimized by particular spin configurations. In the Hopfield model, these minimizing spin configurations constitute the memorized patterns corresponding to the given set of weights w_{ij}. The dynamics of the two networks, starting from an initial condition are very similar.

Combinatorial Optimization Via Single-Electron Dynamics

- We have developed a systematic methodology that determines the C_{ij}'s such that the single-electron computing module solves a number of difficult combinatorial optimization problems including the Traveling Salesman problem.

- The major *limitation* of this model is the requirement that the capacitance (C_{ij}'s) between any two islands is *variable*.

Basic Logic gates
And Circuits
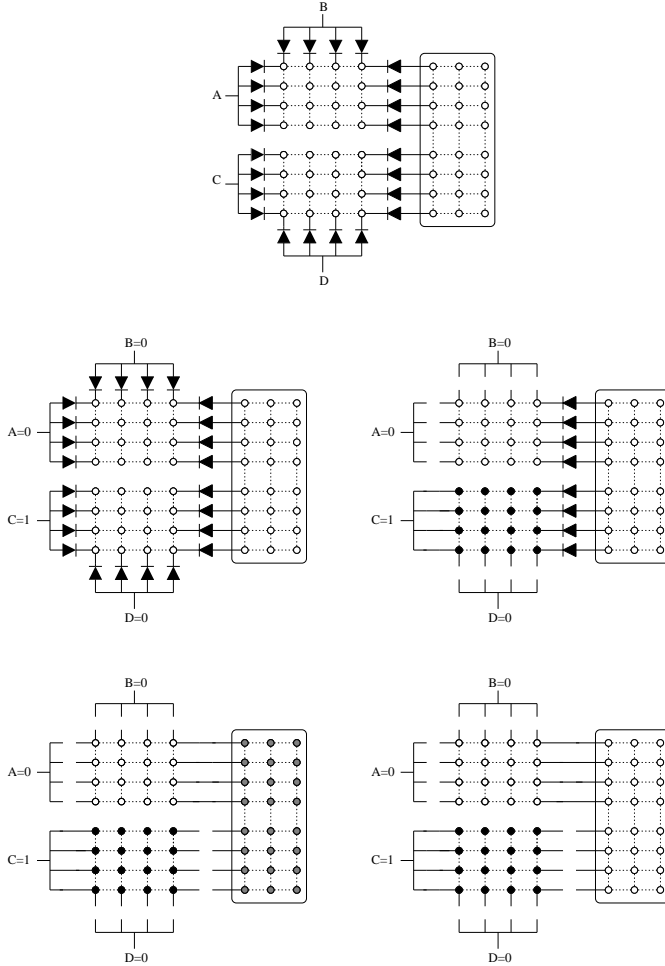
A schematic description of the realization of a 2-level OR/AND circuit using arrays of metallic clusters deposited on a nonohmic layer. *Rectifier* (or *diode*) links delineate gate boundaries. The computation starts by initializing all the individual dots to a low state. This allows the OR gates to complete their respective computations. This step is followed by an initialization of the AND part of the array to a high state. The final state of the AND part will be determined by the already computed states of the OR gates.

Comparison With
Projected 2007 CMOS Technology

	Projected CMOS performance in 2007 [†]		Proposed nanoscale device structures	
	DRAM	LOGIC	20nm Scale	5nm Scale
Minimum feature size (nm)	100	$\sim$ 150 [‡]	20	5
Minimum cell type	DRAM Cell	Logic Transistor	Metal Island	Metal Island
Area of minimum cell (nm^2)	38,000	$\sim$ 1×10^6 [‡]	600	40
Maximum density of computational or storage elements (cells/cm^2)	1.2×10^9	5×10^7	1×10^{11}	1×10^{12}
Power dissipation per unit area (W/cm^2)	–	30	100-500	100-500
Power dissipation per computational cell (nW/cell)	–	600	1-5 [§]	0.1-0.5 [§]

Comparison of Proposed Technology with Projected CMOS Performance Levels.
[†] **Source:** *The National Technology Roadmap For Semiconductors*, **published by the Semiconductor Industry Association.**
[‡] **Figures not given in Roadmap; estimated from available information.**
[§] **Static power estimates used for nanoscale devices.**

Our scheme provides **2-3 orders of magnitude increase in density and speed over the projected CMOS performance.**

Concluding Remarks

- We have provided a <u>novel</u> paradigm for nanoelectronic computation and demonstrated that quantum dots and devices can be used to provide unprecedented increase in computational power.

- We are currently pursuing implementation of our architecture using self-assembly technology where arrays of quantum dots (each 4-10 nm in diameter) are fabricated and are interconnected by molecular wires. The experimental effort is a joint work with groups at Purdue University, Notre Dame University, University of Nebraska-Lincoln, and UCLA.